

FIG. 5

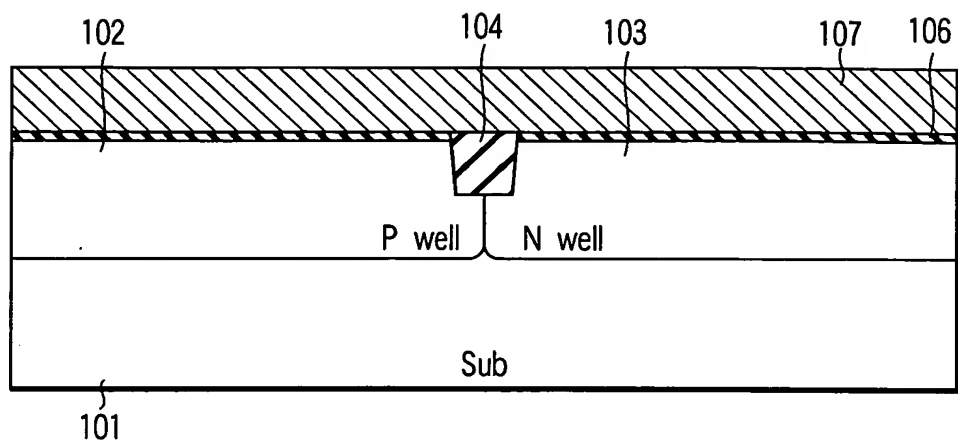


FIG. 6

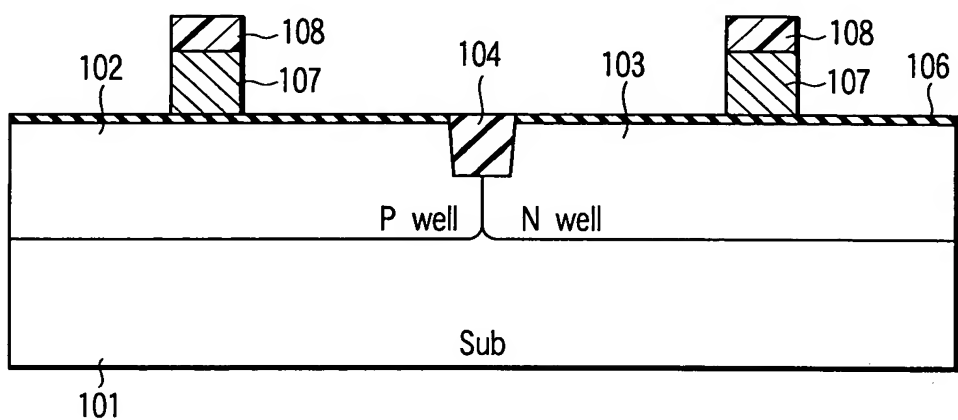


FIG. 7

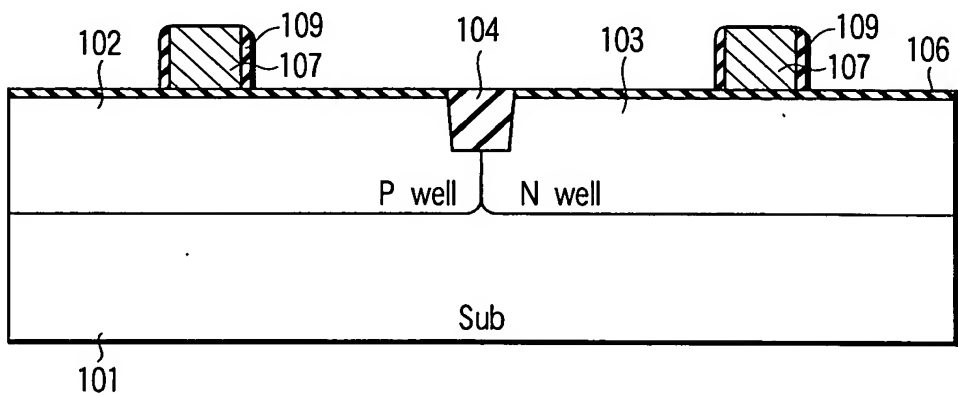
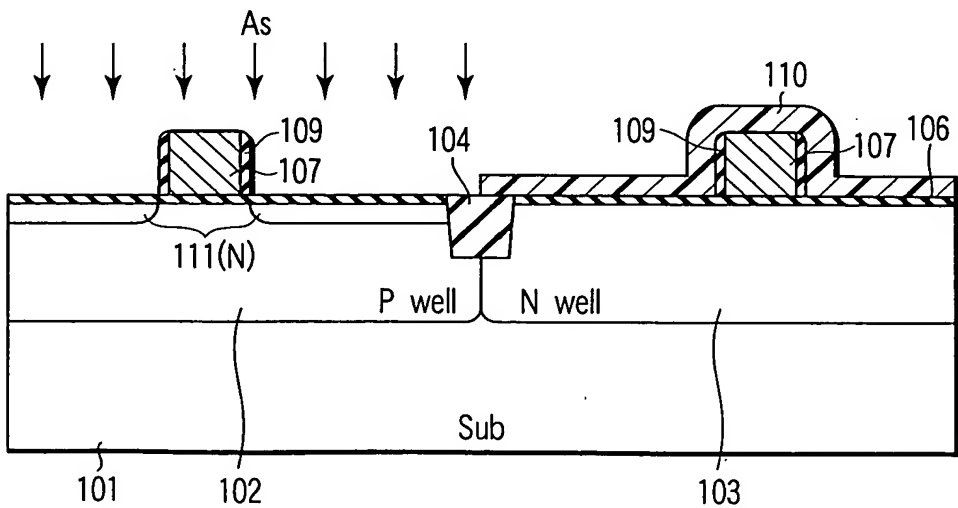


FIG. 8



A cross-sectional view of a semiconductor device. The substrate is labeled 'Sub' and is divided into a 'P well' and an 'N well'. The P well contains a P-type region 111(N) and an N-type region 112(P). The N well contains a P-type region 112(P) and an N-type region 111(N). The device features a gate stack 104 on the P well and a gate stack 106 on the N well. The gate stack 104 includes a gate oxide 109, a gate dielectric 107, and a gate electrode 110'. The gate stack 106 includes a gate oxide 109, a gate dielectric 107, and a gate electrode 110. The device is surrounded by a protective layer 101. The device is labeled 102 and 103.

This cross-sectional view shows a semiconductor device with a central N well (104) and two side P wells (111(N) and 112(P)). The device is built on a substrate (Sub) with regions 101, 102, and 103. A central region 104 is an N well, while the side regions 111(N) and 112(P) are P wells. The top surface is covered by a layer 113, with a central opening 114. Two contact structures (109, 107) are located on the side P wells. A layer 106 is on the right side.

A cross-sectional view of a semiconductor device. The device is divided into three sections labeled 101, 102, and 103. The substrate (Sub) contains a P well and an N well. The central region (102) features a channel region (104) with a gate stack (107, 109). The side regions (101 and 103) feature gate stacks (113, 114) and are labeled 111(N) and 112(P) respectively. The device is also labeled with 106 and 107.

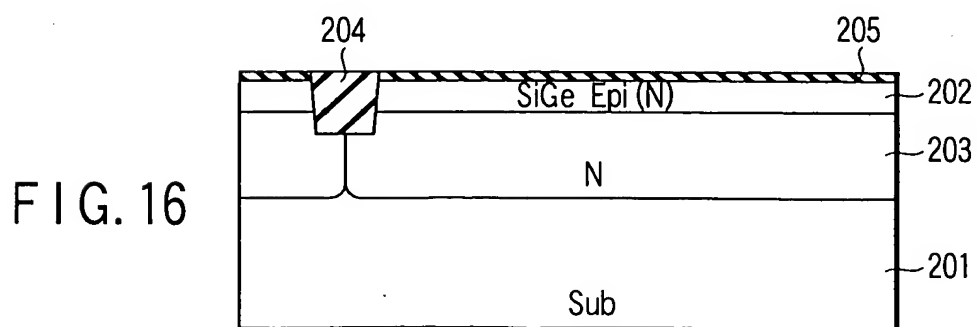
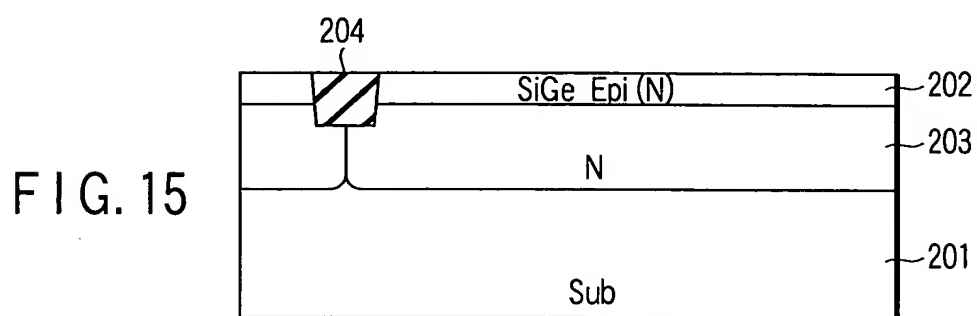
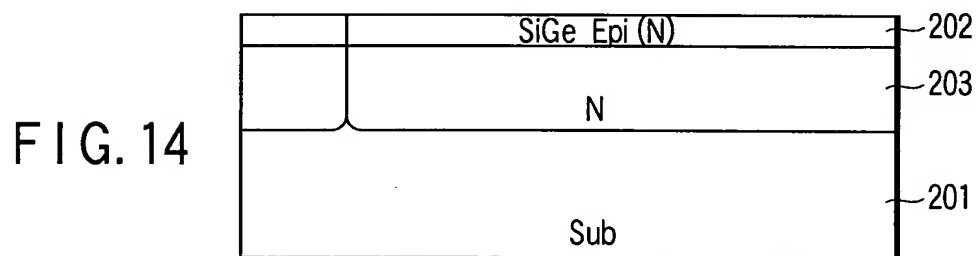
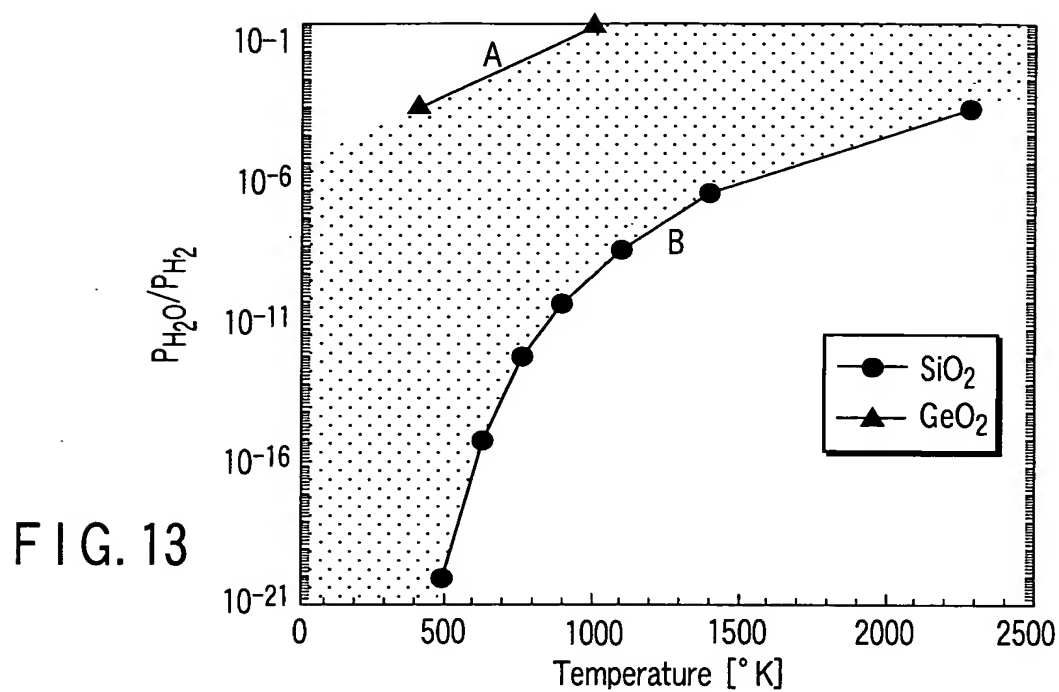


FIG. 17

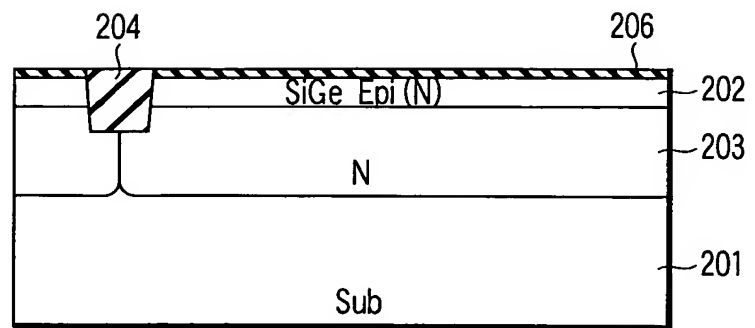


FIG. 18

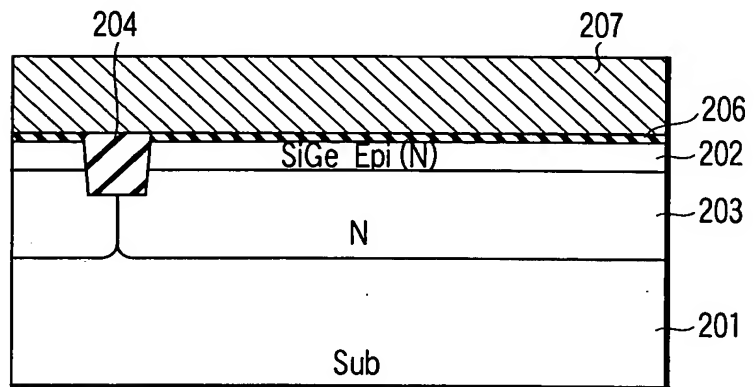


FIG. 19

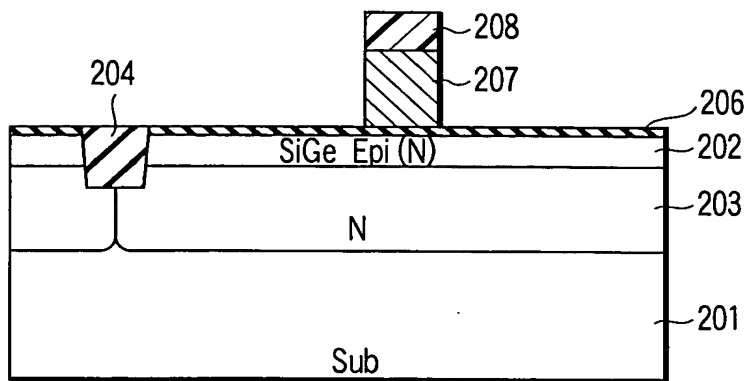


FIG. 20

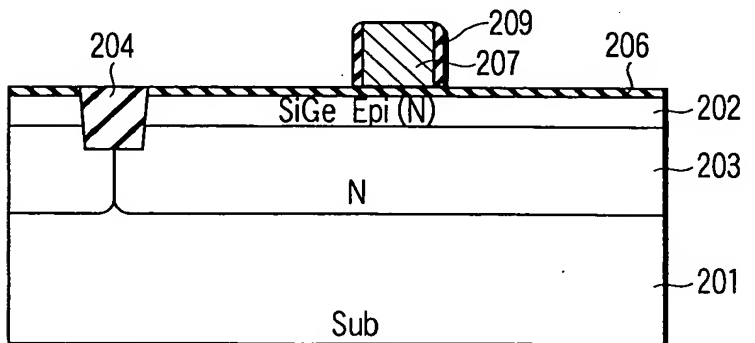


FIG. 21

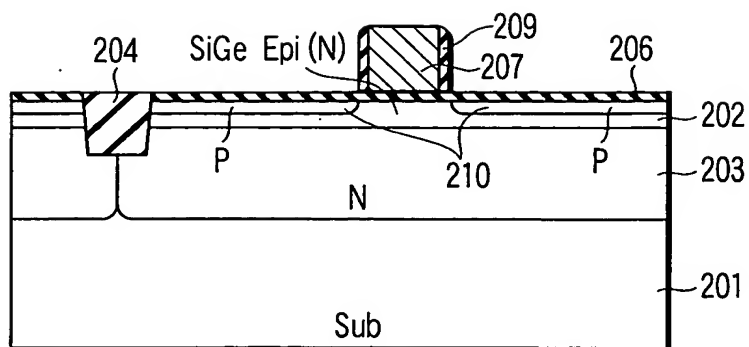


FIG. 22

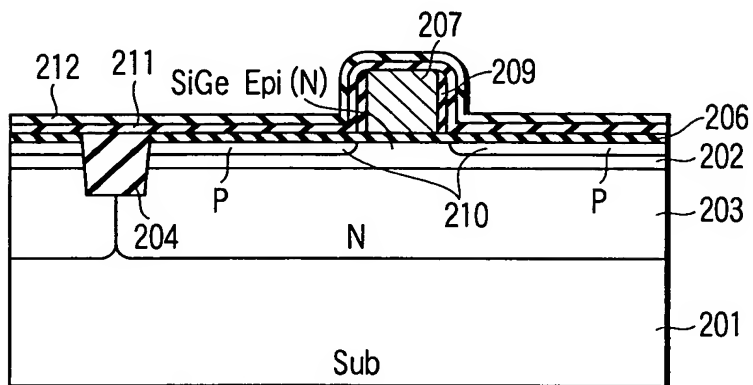


FIG. 23

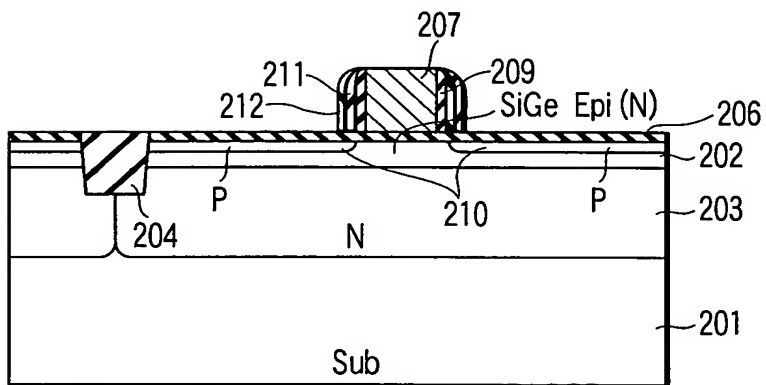
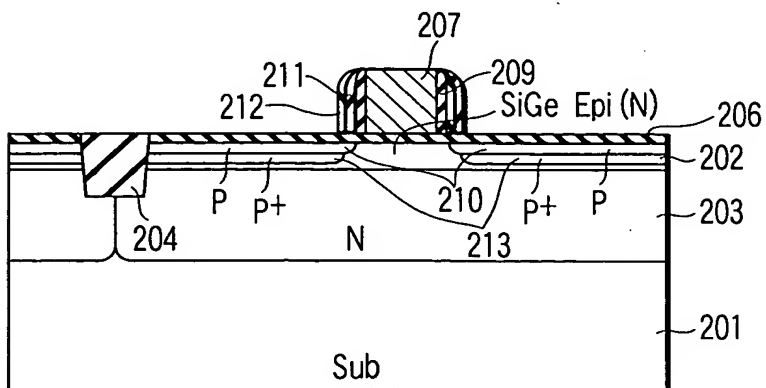


FIG. 24



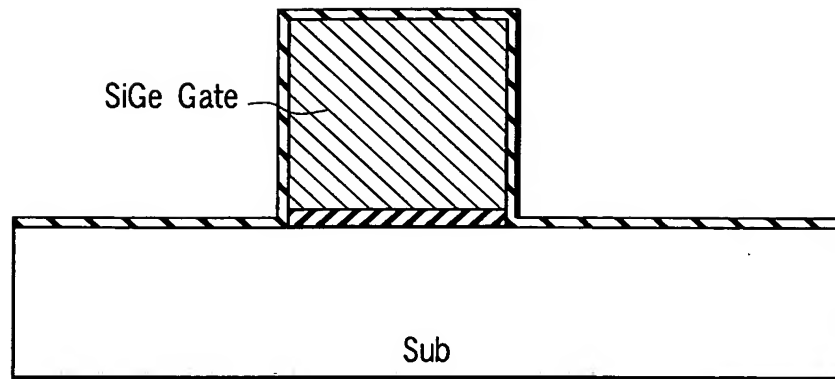


FIG. 25

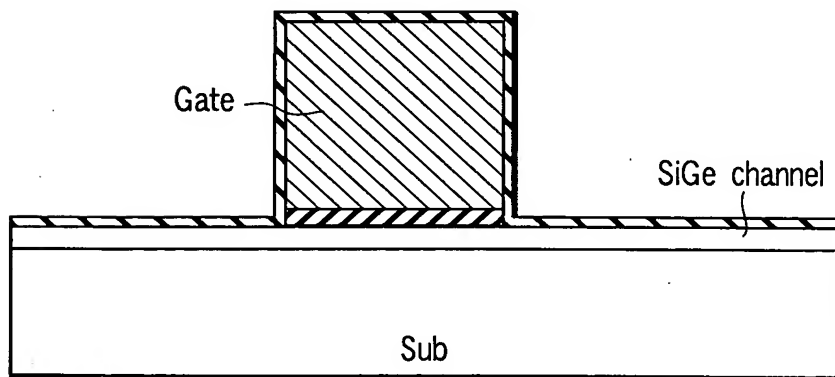


FIG. 26